Sierra Components, Inc.

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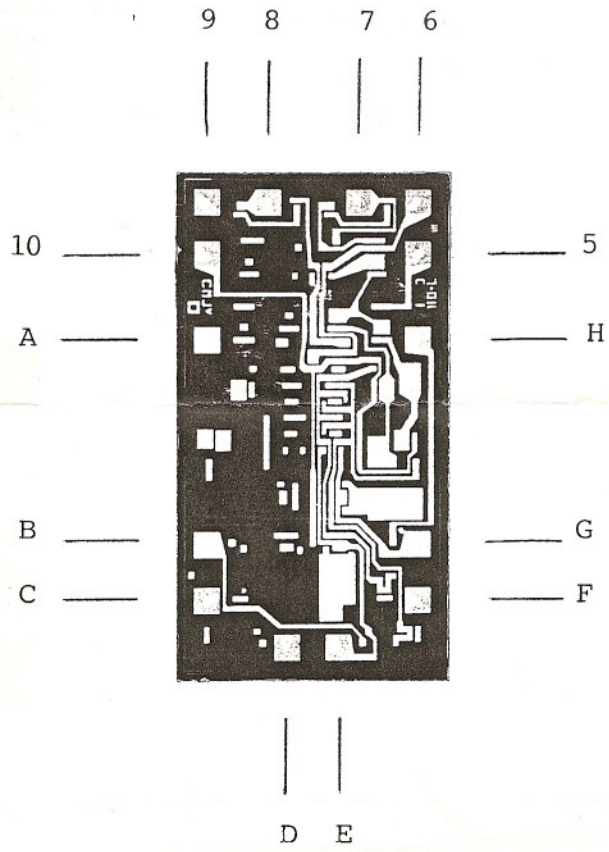
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

STANDARD PACKAGE:



Metal Print: CMJV
7.011
C 1

INTERCHIP PAD CONNECTIONS	
A	Not Connected
B	From JFET 2, Source
C	Not Connected
D	Not Connected
E	To JFET 2, Gate
F	Not Connected
G	To JFET 1, Gate
H	From JFET 1, Source

PAD NO.	FUNCTION
5	Input 1
6	V+
7	V_L
8	V_R
9	Not Connected
10	V- (Substrate)

CMJC1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG186	NIP1000	2
DG187	NC1000	2
DG188	NC2000	2

Topside Metal:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

SIZE: 1.12 x 2.03 m.m.
44 x 80 mils.

APPROVED BY:
MFG: Siliconix

DIE SIZE (Mils): 44 x 80
THICKNESS:

DATE: 3/17/00
P/N: CMJC1000